REMARKS

Examiner:

Claims 1-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over the admitted prior art in view of Klein (Pat. No.6,349,051).

The prior art in Fig.1 [admitted prior art], however, fails to teach that the integrated chipset has a pair of general purpose input/output (GPIO) terminals for outputting a first and second control output; and a pair of switches for respectfully receiving the first access control signal and the second access control signal and selectively outputting the first access control signal and the second access control signal to the three access control mode input ports respectively according to the first control output and the second control output.

It would be obvious to a person of ordinary skill in the art at the time the invention was made to insert a switching device having a reasonable number of switches (e.g. one or two) in the data path of the access control mode input ports of the memory module socket of the admitted prior art in order to reduce the parasitic capacitance of the data bus and increase the speed of data transfer (Klein col.2, lines 52-54). It follows that this modification would necessitate controls signals for the switching device. It is common practice in the art to use the GPIO terminals of many commercially available integrated chipsets to provide these control signals.

Response:

Claims 4-7 have been amended as required by the Examiner.

Klein discloses a device for specifically creating a high-speed bus between a processor circuit and a memory array (Col.1, lines 14-16). The invention teaches a method that aims at increasing data transfer rates by reducing parasitic capacitance between multiple bus lines (Col.1, lines 40-45). The disclosed solution to this problem

is to use one or more switches associated with memory modules to enable a bus line connected to a currently needed memory module while disabling bus lines to memory modules that are not currently needed. "Selective operation of these switches reduces parasitic capacitance of a data bus, and thereby allows increase in the speed data transfer" (Col.2, lines 50-55).

Referring specifically to Examiner cited Fig.4, "a bus switch 27 which splits a single input data bus 31a from the memory controller into a plurality of output data buses 31c, 31d, 31e, 31f which are routed to the respective memory modules 35" Col.4, lines 58-61). As shown in FIG. 4, the memory controller 23 may include a control output 37 which controls the bus switch 27 so as to connect the input data bus 31a to one of the output buses 31c, 31d, 31e, and 31f while the remaining three output buses remain disconnected from the input bus (Col.5, lines 9-13).

The difference between the embodiment shown in Fig.4 and a conventional computer having a plurality of memory modules is obvious. In the conventional computer, all data buses are simultaneously active, resulting in parasitic capacitance. In Fig.4, the switch actives only one of the buses at a time. This is in line with Klein's stated goal of increasing speed by reducing parasitic capacitance. If three of the four buses are disabled, parasitic capacitance should be reduced.

On the other hand, the present invention is directed toward a completely different problem: a management system for access control modes of a single DRAM module socket (Paragraph [0002]). The disclosure states the prior art problem as follows: "For example, ECC mode functionality is supported by a north bridge chip, whereas STR mode functionality is provided by the BIOS. Motherboard support for these functions are determined by adjustments made to the motherboard hardware. For example, to support STR technology, one must switch off related jumpers on the motherboard, and then select STR support when configuring the BIOS" (Paragraph [0006]). "To enable any one of the three access control mode configurations indicated above, the motherboard must be appropriately wired to support the desired configuration. Selection of the access control mode configurations is thus not flexible, and requires

physical changes to the hardware to effect a configuration change" (Paragraph [0009]).

In other words, the present invention management system utilizes software to directly control a desired combination of the access control modes for a DRAM module, and thus does not require any physical reconfiguration of the hardware of a motherboard to effect such access control mode re-configurations (Paragraph [0026]).

With this in mind, it is difficult for the Applicant to understand how the suggested Klein motive of installing a switch to reduce parasitic capacitance and thereby speed data transfers could possibly apply to the admitted prior art. Because the admitted prior art requires physical reconfiguration of the hardware to enable the appropriate data bus for the desired configuration, via jumpers or otherwise, it would seem obvious that the buses not required for a specific configuration are not enabled, unless user enabled by the physical hardware change. Therefore, the admitted prior art already reduces parasitic capacitance as effectively and in much the same manner as the switch of Klein by necessitating the physical reconfiguration of the hardware. Thus, there is no reason for a suggested combination that merely results in unwanted and unnecessary redundancy.

While reducing parasitic capacitance to speed data transfer may be an admirable goal in another system or situation, the prior art disclosure merely solves a problem that is not present in the admitted prior art, and as such, the solution is not applicable. MPEP 2143.01 clearly states that the mere fact that references can be combined or modified to meet claim limitations is not sufficient to establish Prima Facie obviousness unless the prior art also suggests the desirability of the combination. The Applicant contends that the prior art contains no suggestion of the desirability of the combination because, if the unneeded buses of the admitted prior art are hardware disabled and only the desired bus is hardware enabled, not only is parasitic capacitance not a problem in the admitted prior art, but also installing the switch of Klein would be an expensive, unwanted, and unnecessary redundancy.

The inventive step disclosed by the current application is not merely installing a switch into the admitted prior art, although a switch is a necessity. The inventive step is the elimination of the need for hardware reconfiguration every time that a user wishes to reconfigure a plurality of access control modes of a DRAM module. This is accomplished (claim 1) by (a) storing an access control program in BIOS, (b) using a chipset that has a pair of general purpose input/output (GPIO) terminals and a pair of access control mode output ports, (c) using a DRAM module socket that has three access control mode input ports, and (d) using a pair of switches that route access control signals from the chipset to the appropriate access control mode input ports of the DRAM according to control signals received from the chipset. Physical reconfiguration of the hardware is no longer necessary because the user can effectively reconfigure the plurality of access control modes via software in the BIOS. The suggested combination of Klein and admitted prior art neither meets all the claimed structural limitations (e.g. connections from the switch to the access control mode input ports of the DRAM) nor provides any justifiable motivation for the combination.

The Examiner has noted several additional documents as being pertinent to the Applicant's disclosure. These include programmable switching circuitry used to interface with memory modules, using BIOS to control STR or EEC access modes, and use of GPIO terminals of a chipset to control a switch matrix for USB ports. The programmable switching circuitry patents are similar in nature to Klein and fail to anticipate the current application for similar reasons. The patent teaching the use of GPIO terminals to control switching between USB ports fails to meet the claimed structural limitations.

Of some interest are the three patents disclosing the use of BIOS to control either STR or EEC modes. Pat. No. 6,542,996 transfers system memory data in the north bridge to a memory unit under the direction of the south bridge and cuts power to the north bridge according to a signal from BIOS to control STR mode. Pat. No. 5,978,952 discloses time-distributed ECC scrubbing to correct memory errors. Pat. No. 6,212,631 discloses three user-selectable options including L2 cache ECC ON, L2

cache ECC OFF, and L2 cache AUTO. However, none of the cited patents permit a user to select from a plurality of access control modes via software in the BIOS nor meet nor suggest the claimed structural limitations.

As such, the Applicant believes that the present invention is structurally and functionally distinct from all known prior art and respectfully requests reconsideration and allowance of claims 1-7.

Additionally the Applicant requests consideration of new claim 8. Support for the new claim can be found in Figs.4-6. No new material has been introduced.

Sincerely yours,

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